Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (presently amended) A method for multiplying the frame rate of an input video signal ~~having a line rate f_{Hin} and a frame rate f_{Vin},~~ comprising the steps of:

~~propagating said input video signal through just enough memory to delay~~

simultaneously providing said input video signal to a delay memory and a speed-up up memory to provide a delayed video signal and a speeded up video signal;~~by a fraction of a frame period $1/f_{Vin}$~~;

speeding up said delayed video signal to provide a delayed speeded up input video signal ~~a first line rate faster than f_{Hin}~~;

~~speeding up said input video signal to said a second line rate faster than f_{Hin}~~;

alternately supplying at least a portion of said speeded up video signal and at least a portion of said delayed speeded up video signal ~~sequentially, one line at a time; and,~~

~~writing said sequentially supplied lines into~~ to a liquid crystal display ~~at said faster line rate,~~

~~thereby writing at least some of said lines multiple times within each said frame period~~.

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2. (presently amended) The method of claim 1, wherein the step of delaying said input video signal includes ~~comprising the steps~~ a step of storing said input video in a delay memory.~~;~~

~~supplying a plurality of delayed output video signals; and,~~

~~speeding up each of said plurality of delayed video signals to said first and second faster line rates; and,~~

~~sequentially supplying all of said speeded up video signals for said writing step~~.

3. (presently amended) The method of claim 1, comprising the steps of:

periodically interrupting said supplying step to supply a number of consecutive lines of said speeded up video signal;

periodically interrupting said supplying step to supply a number of consecutive lines of said delayed speeded up video signal; and,

alternating said interrupting steps to maintain a uniform time interval between writing lines into ~~the~~ a same line-number position on said liquid crystal display.

4. (presently amended) The method of claim 1, wherein said step of alternately supplying said video signal comprises a ~~comprising~~ the step of alternately writing lines of said video signal to ~~a~~ said liquid crystal on silicon display.

B' cont'd

5. (canceled)

6. (presently amended) The method of claim ~~1~~2, ~~comprising the step of propagating said input video signal through just enough~~ wherein the step of storing said video in said delay memory is carried out by storing less than a full frame of video in said delay memory. ~~to delay said input video signal by (n-1)/n of said frame period, where n is a multiplication factor of said frame multiplying.~~

7. (presently amended) The method of claim 1, comprising the steps of:

at least doubling said frame rate of said input video signal; and,

writing ~~each of said~~ selected lines of said video signal multiple times to said liquid crystal display.

8. (presently amended) The method of claim 1, comprising the step of speeding up said delayed video signal and said input video signal to the same line rate. ~~faster than f_{Hin}.~~

9. (presently amended) A method for ~~doubling~~ multiplying the frame rate of ~~an input~~ a video signal ~~having a line rate f_{Hin} and a frame rate f_{Vin},~~ comprising the steps of:

~~propagating said input video signal through just enough memory to delay~~ delaying said input video signal ~~by 1/2 of~~ for a time less than one ~~a~~ frame period ~~$1/f_{Vin}$~~;

speeding up said delayed video signal ~~to a first line rate faster than f_{Hin}~~;

speeding up said input video signal ~~to a second line rate faster than f_{Hin}~~;

alternately supplying lines of said speeded up video signal and lines of said delayed speeded up video signal ~~sequentially, one line at a time~~; and,

writing said ~~sequentially~~ alternately supplied lines into a liquid crystal display ~~at said faster line rate,~~

~~thereby writing each of said lines twice within each said frame period~~.

10. (original) The method of claim 9, comprising the steps of:

periodically interrupting said supplying step to supply a number of consecutive lines of said speeded up video signal;

periodically interrupting said supplying step to supply a number of consecutive lines of said delayed speeded up video signal; and,

alternating said interrupting steps to maintain a uniform time interval between writing lines into the same line-number position on said liquid crystal display.

11. (original) The method of claim 9, comprising the step of simultaneously writing said lines to top and bottom halves of said ~~a liquid crystal on silicon~~ display.

12. (original) The method of claim 9, comprising the step of propagating said input video signal through a memory embedded in an integrated circuit.

13. (original) The method of claim 9, comprising the step of speeding up said delayed video signal and said input video signal to the same line rate. ~~of $2f_{Hin}$~~.

14. (presently amended) A frame rate multiplier for an input video signal ~~having a line rate f_{Hin} and a frame rate f_{Vin}, said frame rate multiplier~~ comprising:

a ~~first~~ delay memory and a first speed up memory for receiving said input video signal, ~~said first memory having a maximum required data storage capacity just large enough to delay said input video signal for a fraction of a frame period $1/f_{Vin}$~~;

a second speed up memory coupled to an output of said delay memory for speeding up said delayed video signal; ~~to a first line rate faster than f_{Hin};~~

~~a third memory for receiving speeding up said input video signal to a second line rate faster than f_{Hin};~~

a multiplexer coupled to said first and second speed up memories; ~~for receiving both said speeded up video signals and supplying said speeded up video signals one line at a time for writing to a liquid crystal display, and,~~

a display coupled to said multiplexer ;

~~a source of clock signals and control signals, said source being coupled to each of said memories, to said multiplexer and to said liquid crystal display,~~ such that ~~successive lines~~ portions of video supplied by said multiplexer to said ~~liquid crystal~~ display originate alternately from said first and second ~~and third~~ speed up memories ~~at said faster line rates, at least some of said supplied lines being supplied to said liquid crystal display multiple times within each said frame period~~.

B' cont'd

15. (presently amended) The frame rate multiplier of claim 14, wherein said delay memory comprises a partial frame memory storing ~~a maximum required data storage capacity of said first memory is~~ less than ~~(n-1)/n of a~~ one frame of said video signal, ~~where n is the multiplication factor of said frame rate multiplier~~.

16. (presently amended) The frame rate multiplier of claim ~~15~~ 14, wherein said ~~first~~ speed up memory comprises an array of ~~has n-1~~ speed up memories. ~~outputs for supplying n-1 delayed output video signals, where n ≥ 2.~~

17. (presently amended) The frame rate multiplier of claim ~~16~~ 14 wherein said delay memory comprises an array of ~~comprising n-1~~ memories. ~~coupled to said first memory and to said multiplexer for speeding up said n-1 delayed output video signals to said faster line rates; and,~~

~~said lines supplied by said multiplexer to said liquid crystal display originating sequentially from said third memory and said n-1 memories~~.

18. (canceled)

19. (canceled)

20. (presently amended) The frame rate multiplier of claim 14, wherein said ~~first~~ delay memory and said first speed up memory ~~second memories are functionally combined into~~ comprise a single memory ~~to both delay and speed up said input video signal~~.

21. (presently amended) The frame rate multiplier of claim 14, wherein said ~~first~~ delay memory and said ~~,~~ first and second ~~and third~~ speed up memories ~~are functionally combined into~~ comprise a single memory ~~to delay and speed up said delayed input video signal and to speed up said input video signal~~.

22. (canceled)

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23. (presently amended) A frame rate doubler ~~for an input video signal having a line rate f_{Hin} and a frame rate f_{Vin}, said frame rate doubler~~ comprising:

a first memory for delaying said input video signal ~~for $1/2$ of a frame period $1/f_{Vin}$~~;

a second memory for speeding up said delayed video signal ~~to a line rate faster than f_{Hin}~~;

a third memory for speeding up said input video signal ~~to a second line rate faster than f_{Hin}~~;

a multiplexer coupled ~~for receiving both said speeded up video signals and~~ to said second and third memories so as to alternately select ~~supplying said speeded up~~ video signals ~~one line at a time~~ output from said second and third memories for writing to a liquid crystal display~~, and~~,

~~a source of clock signals and control signals, said source being coupled to each of said memories, to said multiplexer and to said liquid crystal display, such that successive lines supplied by said multiplexer to said liquid crystal display originate alternately from said second and third memories at said faster line rate, each of said supplied line being supplied to said liquid crystal display twice within each said frame period~~.

24. (presently amended) The frame rate doubler of claim 23, wherein said first memory stores not more than about ~~has a maximum required data storage capacity of~~ $1/2$ of a frame said video signal.

25. (presently amended) The frame rate doubler of claim 23, ~~wherein said~~ further comprising a controller coupled to said second and third memories and programmed to:~~source of clock signals and control signals provides providing an operating mode in which said multiplexer is controlled to~~:

periodically interrupt said supply of said ~~lines~~ video portions to said liquid crystal display;

supply to said liquid crystal display during said periodic interruptions n successive lines from at least one of said second ~~memory~~ and third memories ~~or n successive lines from said third memory; and,alternately select said n successive lines from said second or third memory in order~~ so as to maintain a uniform time interval between writing lines into ~~the~~ a same line-number position on said liquid crystal display.

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26. (original) The frame rate doubler of claim 23, wherein said liquid crystal display comprises liquid crystal on silicon.

27. (canceled)

28. (canceled)

29. (presently amended) The frame rate doubler of claim 23, wherein said first and second memories are functionally combined into a single memory,~~to both delay and speed up said input video signal.~~

30. (canceled)

31. (canceled)

32. (new) The method of claim 1 including a step of storing in said delay memory not more than a portion of said input signal approximately equal to 1/n of a frame of said input video signal, wherein n represents a multiplying factor for said frame rate multiplier.

33. (new) The frame rate multiplier of claim 14 further comprising a controller coupled to said multiplexer such that said multiplexer is controlled to alternately select a number of successive lines from said first and second speed up memories so as to maintain a

B' cancel.

uniform time interval between writing lines into the same line-number position on said liquid crystal display.